IN THE CLAIMS

1. (Currently amended) A digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, and control means for controlling said functional units, characterized in that said control means comprises a fetch unit, a decode unit, and a plurality of control units responsive to said decode unit, wherein at least one control unit is operatively associated with a respective functional unit for controlling its function, including controlling a number of repetitions of execution of its function, and each functional unit is adapted to execute operations in an autonomous manner under control of the control unit associated therewith.

2. (Currently amended) An apparatus according to claim 1, characterized by FIFO (first-in/fist-out) register means adapted for supporting data-flow communication among said functional units.

3. (Previously presented) A digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, and control means for controlling said functional units in coordination with one another in response to a single fetch unit and a single decode unit, characterized by FIFO (first-in/fist-out) register means adapted for supporting data-flow communication among said functional units.

4. (Cancel)

5. (Previously presented) Apparatus according to any one of claims 2, characterized in that said FIFO register means comprises a plurality of FIFO registers.

6. (Currently amended) An apparatus according to claim 1, characterized in that each of said functional units are provided with at least one control unit.

7. (Currently amended) An apparatus according to claim 1, which apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage ~~is executed by~~comprises a functional unit.

8. (Currently amended) An apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, where-in said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit .

9. (Currently amended) An apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units.

10. (Currently amended) A method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units wherein each functional

unit is adapted to execute operations, characterized in that said functional units are controlled by control means including a single fetch unit, a single decode unit and a plurality of control units wherein at least one control unit is operatively associated with a respective unit so that each functional unit is able to execute operations in an autonomous manner under control of the control unit associated therewith, the control unit controlling a number of repetitions of execution of its associated functional unit.

11. (Currently amended) An apparatus according to claim 9, characterized in that data-flow communication among said functional units is supported by FIFO (first-in/first-out) register means .

12. (Canceled)

13. (Currently amended) An apparatus according to claim 11, wherein a pipeline consisting of a plurality of stages is provided, and each stage is executed by a functional unit .

14. (Currently amended) An apparatus according to claim 10, characterized in that the number of times an instruction stored has to be executed by a functional unit is counted by the corresponding control unit .

15. (Cancel)